



AF ZMW

PTO/SB/21 (09-04)

Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

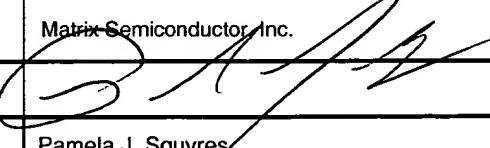
Total Number of Pages in This Submission

31

Application Number	09/918,853
Filing Date	July 30, 2001
First Named Inventor	Michael A Vydova
Art Unit	2823
Examiner Name	Fernando L. Toledo
Attorney Docket Number	MA-046

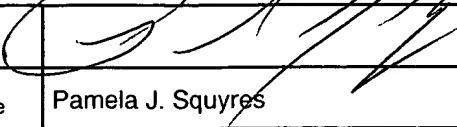
ENCLOSURES (Check all that apply)		
<input type="checkbox"/> Fee Transmittal Form	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> After Allowance Communication to TC
<input type="checkbox"/> Fee Attached	<input type="checkbox"/> Licensing-related Papers	<input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences
<input type="checkbox"/> Amendment/Reply	<input type="checkbox"/> Petition	<input checked="" type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
<input type="checkbox"/> After Final	<input type="checkbox"/> Petition to Convert to a Provisional Application	<input type="checkbox"/> Proprietary Information
<input type="checkbox"/> Affidavits/declaration(s)	<input type="checkbox"/> Power of Attorney, Revocation	<input type="checkbox"/> Status Letter
<input type="checkbox"/> Extension of Time Request	<input type="checkbox"/> Change of Correspondence Address	<input checked="" type="checkbox"/> Other Enclosure(s) (please identify below):
<input type="checkbox"/> Express Abandonment Request	<input type="checkbox"/> Terminal Disclaimer	<input type="checkbox"/> Return receipt postcard
<input type="checkbox"/> Information Disclosure Statement	<input type="checkbox"/> Request for Refund	
<input type="checkbox"/> Certified Copy of Priority Document(s)	<input type="checkbox"/> CD, Number of CD(s) _____	
<input type="checkbox"/> Reply to Missing Parts/ Incomplete Application	<input type="checkbox"/> Landscape Table on CD	
<input type="checkbox"/> <input type="checkbox"/> Reply to Missing Parts under 37 CFR 1.52 or 1.53		
Remarks		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Matrix Semiconductor, Inc.		
Signature			
Printed name	Pamela J. Squyres		
Date	Dec. 13, 2005	Reg. No.	52246

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature			
Typed or printed name	Pamela J. Squyres	Date	Dec. 13, 2005

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No. MA-046

In re patent application of
Michael A. Vyvoda et al.

Serial No. 09/918,853

Group Art Unit: 2823

Filed: July 30, 2001

Examiner: Fernando L. Toledo

For: PROCESS FOR FABRICATING A DIELECTRIC FILM USING PLASMA
OXIDATION

REPLACEMENT BRIEF ON APPEAL

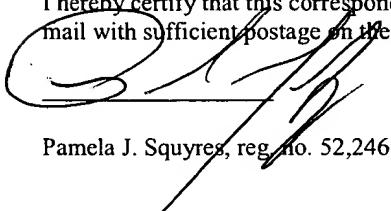
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

December 13, 2005

To the Commissioner:

Appellants hereby appeal the December 14, 2004 final rejection of claims 1-24, 35-40 and 55-153 in the above-identified application to the Board of Patent Appeals and Interferences. This Appeal Brief is resubmitted in response to a Notice of Non-Compliant Appeal Brief.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date below.


Pamela J. Squyres, reg. no. 52,246

Dec. 13, 2005

Date of Deposit

TABLE OF CONTENTS

I. Real Party in Interest.....	3
II. Related Appeals and Interferences.....	4
III. Status of Claims.....	5
IV. Status of Amendments.....	6
V. Summary of Claimed Subject Matter.....	7
VI. Grounds of Rejection to be Reviewed on Appeal.....	8
VII. Arguments.....	9
VIII. Claims Appendix.....	18
IX. Evidence Appendix.....	35
X. Related Proceedings Appendix.....	36

I. REAL PARTY IN INTEREST

The real party in interest is Matrix Semiconductor, Inc., a Delaware corporation.

II. RELATED APPEALS AND INTERFERENCES

The undersigned is not aware of other related appeals and interferences.

III. STATUS OF CLAIMS

Claims 1-153 are pending in the Application. Claims 25-34 and 41-54 are withdrawn from consideration. A listing of the appealed claims is presented in the APPENDIX.

Claims 1-153 are pending. Claims 25-34 and 41-54 have been withdrawn from consideration. Claims 1-24, 35-40, and 55-153 have been rejected. Claims 1-24, 35-40, and 55-153 are the subject of this appeal.

IV. STATUS OF AMENDMENTS

No amendments after final rejection were filed.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Non-conductive oxides, especially silicon dioxide, are widely used in semiconductor devices as interlevel dielectric, gap fill, gate dielectrics, and serving many other roles.

Silicon dioxide can be deposited, but can also be grown from silicon, which is widely used in semiconductor devices, by exposing it to an oxidation process. Silicon dioxide is a high-quality dielectric.

The conventional way to grow oxide is by thermal oxidation. Thermal oxidation, however, requires relatively high temperatures, which may cause unwanted dopant diffusion and other undesired changes in the device.

In the present invention a high density plasma oxidation process is provided in which the plasma activity is regulated to control the rate of oxidation. Plasma oxidation conditions are provided such that the growth rate of the dielectric film is limited in order to produce a dielectric layer having a precise thickness and uniformity. The high density plasma oxidation process can be used to fabricate gate oxide layers, passivation layers and antifuse layers in semiconductor devices such as semiconductor memory devices and multi-level memory arrays.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following grounds of rejection are to be reviewed on appeal:

- 1) Whether claims 113-117, 119, 122-124, 126, 128, 130-132, 134-140, 142-145 and 147-153 are anticipated by Thomas, US Patent No. 6,509,283, under 35 USC 102(e), hereinafter “Thomas”.
- 2) Whether claims 1-5, 7, 10-12, 14, 16, 18-20, 22-24, 35, 38-40, 55-58, 60-63, and 65-71 are unpatentable under 35 USC 103(a) over Thomas in view of Moon et al., US Patent Publication No. 2002/0137266, hereinafter “Moon et al.”
- 3) Whether claims 72-76, 78, 81-83, 85, 87, 89-91, 93-99, 101-104 and 106-112 are unpatentable under 35 USC 103(a) over Thomas in view of Chung et al., US Patent No. 5,930,650, hereinafter “Chung et al.”

VII. ARGUMENT

I. Claims 113, 130, 137, 144, and 149 are not anticipated by Thomas

Independent claims 113, 130, 137, 144, and 149 were rejected under 35 USC 102(e) as being anticipated by Thomas. Claim 113 recites a plasma oxidation process comprising exposing an oxidizable surface to an oxidizing plasma, wherein the oxidizing plasma has an activity relative to the oxidizable surface; forming an oxide film on the oxidizable surface; and regulating the oxidizing plasma activity to limit a rate of formation of the oxide film to a predetermined growth rate while the oxidizable surface is being exposed to the oxidizing plasma.

Appellants will show that Thomas teaches neither plasma oxidation nor limiting of rate of formation of oxide by regulating plasma activity.

I.a. Thomas does not teach plasma oxidation

Each of the independent claims rejected by this rationale includes the limitation of “exposing an oxidizable surface to an oxidizing plasma” (claim 113), or “exposing the semiconductor layer to a plasma comprising oxygen” (claim 130), or “exposing an oxidizable surface to a plasma comprising an oxygen species” (claim 137 and 149), or “exposing an oxidizable surface to a plasma comprising oxygen” (claim 144).

Appellants respectfully assert that Thomas teaches *thermal* oxidation, but does not show *plasma* oxidation, nor does the reference teach an oxidizable or semiconductor surface exposed to a plasma.

Plasma oxidation processes are typically carried out at temperatures below about 600° C. In comparison, a conventional thermal oxidation process used to form, for example, silicon dioxide is typically carried out at temperatures in excess of 900° C. The present application describes how the lower temperature required by use of a plasma oxidation

process reduces diffusion of dopants in the substrate, which enables the formation of the shallow junctions necessary for high-speed devices.

Thomas teaches a pre-heat to 500° C in the presence of an inert gas to prevent oxidation, then ramping to a second temperature, for example 1000° C, and introducing atomic oxygen to perform oxidation (col. 2, lines 39-52.) No plasma is present during oxidation. The temperature (1000° C) is appropriate for thermal oxidation, not plasma oxidation. Thomas further notes that if “an oxygen/nitrogen mixture is used, then nitrogen-doped *thermal oxide* results.” (Emphasis added.) Indeed the title of the Thomas patent, “Thermal Oxidation Method Utilizing Atomic Oxygen to Reduce Dangling Bonds in Silicon Dioxide Grown on Silicon,” specifies *thermal* oxidation, not plasma oxidation.

A plasma reactor is mentioned by Thomas, but only as a method of generating the atomic oxygen introduced into the chamber for thermal oxidation. Thomas specifies that, rather than being present during oxidation, a plasma is a “remote source” of atomic oxygen, and the atomic oxygen is “then introduced into the furnace chamber containing the silicon to be *thermally oxidized*” (col. 2, lines 1-4, emphasis added; see also col. 3, lines 22-25 and Fig. 3.) That is, a plasma is created in another, remote location. This plasma is used to generate atomic oxygen, and the atomic oxygen, *not* the plasma, is then introduced into the furnace chamber where the *thermal* oxidation of silicon described by Thomas takes place. Nowhere does Thomas describe a plasma present while oxidation takes place, or exposure of the silicon surface to be oxidized to a plasma. A plasma is an ionized gas, while atomic oxygen is oxygen in its atomic form, rather than its more common molecular form (O₂).

In the final rejection of December 14, 2004, the Examiner continues to maintain that Thomas teaches plasma oxidation, citing the following passage in Thomas (col. 3, lines 25-41):

As shown in FIG. 3, furnace 52 includes a reactor vessel 54 and controlled heating elements 56, as described above. As in the previous embodiment, the reactor vessel 54 is adapted to hold a plurality of wafers 58 having an exposed silicon surface. In this embodiment, however, rather than the atomic oxygen (or atomic oxygen plus atomic nitrogen) being generated within the reactor vessel 54, a remote source 60, e.g., a plasma reactor, generates a flow 62 of atomic oxygen (or O₋ +N⁻) which is provided to the vessel 54. The furnace heats the wafers 58 to a temperature suitable for reaction of the silicon and atomic oxygen (or O₋ +N⁻) to form silicon dioxide (or nitrogen-doped SiO₂).

Those skilled in the art will appreciate that the FIG. 3 embodiment of the invention can be supplemented with a source 64 of atomic chlorine, generated either remotely (e.g., chlorine plasma) or within the vessel 54 using a ceramic material in the manner described above in conjunction with the FIG. 2 embodiment of the invention. (Emphasis added.)

In interpreting this passage, the Examiner argues (p. 34, paragraph 127 of the December 14, 2004 Office Action):

... Thomas forms the oxygen plasma at a remote location and then drives it to where the wafer (or wafers) is, to form the SiO_x layer.

Appellants respectfully suggest that the Examiner has misinterpreted the cited passage in Thomas. The Examiner maintains that a plasma is generated remotely, then the plasma is driven to the wafer. On a careful read, however, it becomes clear that a plasma reactor is used to generate “a flow of atomic oxygen”, and the atomic oxygen, *not a plasma*, is then driven to the chamber. To reiterate, atomic oxygen is not the same as an oxygen plasma. The oxidizable surface is exposed *to the atomic oxygen which was formed in the plasma reactor*, but never at any point to an actual plasma.

I.b. Thomas does not teach regulation of plasma activity to limit rate of formation of oxide

In addition, each of the independent claims rejected by this rationale includes the limitation of “regulating the oxidizing plasma activity to limit a rate of formation of the oxide film” (claim 113), or “regulating the plasma activity to limit a rate of formation of the oxide film,” (claims 130 and 144), or “regulating the plasma activity to limit a rate of formation of the oxynitride film,” (claim 137), or “regulating the plasma activity to limit a rate of

formation of the oxide film to a predetermined growth rate while the oxidizable surface is being exposed to the plasma,” (claim 149).

Appellants can find no teaching in Thomas of regulating the oxidizing plasma activity to limit a rate of formation of the oxide film to a predetermined growth rate while the oxidizable surface is being exposed to the oxidizing plasma, nor has the Examiner identified any such teaching. Indeed, as the oxidizable surface is at no point exposed to a plasma, no such teaching could exist. The word “plasma” appears in Thomas only in the Abstract, in the Summary, and in col. 3; none of these appearance includes any mention of regulation of plasma activity for any purpose, nor to the rate of oxidation. In fact, Appellants can find no teaching of regulation of rate of oxidation rate in Thomas by *any* method, and the Examiner has identified none.

The response of September 23, 2004, included a declaration under 37 CFR 1.132 in which an inventor of the present invention attests to his opinion that Thomas teaches neither plasma oxidation nor regulation of plasma activity to limit the rate of oxide formation.

Appellants thus respectfully maintain that, as Thomas fails to teach the plasma oxidation and regulation of oxidation rate recited in the rejected claims, Thomas cannot anticipate these claims. Accordingly, Applicants respectfully request that the 102(e) rejections of independent claims 113, 130, 137, 144, and 149 and their dependent claims be withdrawn.

II. Claims 1, 18, 35, 55, and 62 are patentable over the applied references

Independent claims 1, 18, 35, 55, 62, and 67 were rejected under 35 USC 103(a) over Thomas in view of Moon et al. Claim 1 recites a plasma oxidation process comprising exposing an oxidizable surface to an oxidizing plasma, wherein the oxidizing plasma has an activity relative to the oxidizable surface; forming an oxide film on the oxidizable surface;

and regulating the oxidizing plasma activity to limit a rate of formation of the oxide film.

Claim 35 recites a process for forming an antifuse comprising exposing an oxidizable surface to a plasma oxidation process for an initial exposure time; and growing an oxide film on the oxidizable surface, and *wherein the oxide film grows to a predetermined thickness at an end of the initial exposure time, and wherein additional exposure to the plasma oxidation process beyond the initial exposure time does not result in a significant further increase in thickness of the oxide film.*

The Examiner asserts that Thomas discloses plasma oxidation and regulating plasma activity to limit a rate of formation of oxide. As Appellants have earlier shown (in Sections I.a and I.b of these Arguments) there is in fact no disclosure in Thomas of either of these elements.

The Examiner admits that Thomas does not show limiting the oxygen thickness:

Thomas does not show wherein the oxide film grows to a predetermined thickness at an end of an initial exposure time to the oxidizing plasma.

The Examiner then argues that Moon et al. teach that “an oxide layer will not increase substantially beyond an initial exposure time.” Thus in rejecting claims 1, 18, 35, 55, 62, and 67 and their dependents, the Examiner relies on teachings of Moon et al. to show limiting of oxide thickness.

Appellants note that of the independent claims (1, 18, 35, 55, 62, and 67) rejected using the combination of Thomas and Moon et al., only claim 35 actually discusses oxide thickness. The others all refer to limiting *rate of formation* of oxide, and make no mention of oxide thickness. Appellants explained in Section I.b of this Argument that Thomas does not teach limiting the *rate of oxidation*. The Examiner argues only that Moon et al. teach a limit to the thickness of the oxide, not the rate of formation of oxide. Clearly limiting the rate of

formation of oxide is not the same as limiting the ultimate thickness of an oxide; even at a very low oxidation rate, oxide thickness could continue to increase.

Appellants thus maintain that the rejections over Thomas and Moon et al. of claims 1, 18, 55, 62, and 67 should be withdrawn, as the Examiner has not shown, in either Thomas or Moon et al., regulation of the *rate* of oxidation. Appellants will focus on the rejection of claim 35, which does recite limited oxide thickness.

Moon et al. do indeed teach an oxide layer not increasing substantially beyond an initial exposure time. But the oxidation of Moon et al. takes place in air at room temperature (see paragraph [0031]), not in an atomic oxygen atmosphere at 1000° C as in Thomas. There is no reason to expect the extent of oxidation to be similar in these radically different conditions. It is well known that temperature and atmospheric gases dramatically alter the rate and extent of oxidation of silicon; indeed, commercial furnaces exist for this reason. Thus the teachings of Moon et al. have no clear relevance to Thomas, and still less to the plasma oxidation process recited in independent claim 35 and its dependent claims.

Simply put, the fact that a silicon wafer sitting in air at room temperature will oxidize to a certain thickness and no further has no apparent relevance to the progress of thermal oxidation performed at high temperature in a furnace (as in Thomas) or during plasma oxidation (as in the claims.)

Appellants can find no suggestion to combine Thomas or Moon et al. in either reference, nor has the Examiner identified any such suggestion. The extremely different conditions of oxidation would further tend to make one skilled in the art unlikely to make such a combination.

To summarize, the teaching of Moon et al. regarding the tendency of oxide formation to stop at a given thickness *in air at room temperature* has no conceivable relevance to high-

temperature (1000 degrees C) oxidation in a furnace, so there is no motivation to combine the references. In addition, even if the references were combined, the result is not a limit in the thickness of oxide produced by *plasma oxidation*, as recited in the claim, as neither Moon et al. nor Thomas teaches plasma oxidation.

Accordingly, Appellants respectfully request that the rejections of independent claims 1, 18, 35, 55, 62, and 67 and their dependent claims be withdrawn.

III. Claims 72, 89, 96, 103, and 108 patentable over the applied references

Claims 72, 89, 96, 103, and 108 were rejected under 35 USC 103(a) over Thomas in view of Chung et al. Claim 72 recites a plasma oxidation process comprising: exposing an oxidizable surface to an oxidizing plasma, wherein the oxidizing plasma has an activity relative to the oxidizable surface; forming an oxide film on the oxidizable surface; and regulating the oxidizing plasma activity to limit a rate of formation of the oxide film by regulating at least one of the following: reaction kinetics, growth initiation, and surface energy.

Claims 89, 96, 103, and 108 all include similar limitations regarding plasma oxidation or exposure of an oxidizable surface to a plasma comprising oxygen and/or nitrogen species, and regulating plasma activity to limit a rate of formation of the oxide (or oxynitride) film by regulating at least one of the following: reaction kinetics, growth initiation, and surface energy.

The Examiner maintains first that Thomas teaches exposing an oxidizable surface to an oxidizing plasma. Appellants have shown in Section I.a, however, that Thomas teaches exposure to atomic oxygen, not to an oxidizing plasma. The Examiner admits that Thomas does not disclose regulating at least one of reaction kinetics, growth initiation, or surface energy to limit the oxidation rate.

The Examiner then relies on Chung et al.:

Chung ... discloses that reaction kinetics is a process variable of a reaction process (column 3).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to regulate at least one of the following: reaction kinetics, growth initiation and surface energy in the invention of Thomas, since as taught by Chung, reaction kinetics is a process variable and discovering the optimum or workable ranges requires only routine experimentation.

Thomas, as noted, teaches thermal oxidation, while Chung et al. teach an etch process.

Appellants are unable to identify any connection between the process of Thomas and that of Chung et al. An etch process is not an oxidation process, and the processes do not occur in similar devices or under similar conditions. No apparent motivation exists for one skilled in the art to apply the teachings of Chung et al. to Thomas.

To summarize, neither cited reference teaches plasma oxidation, as recited in the claims. Neither cited reference teaches regulation of the rate of oxidation, as recited in the claims. Chung et al. discuss reaction kinetics relative to an etch process. Appellants cannot see how one skilled in the art could a) take a teaching that reaction kinetics is a process variable of a reaction process relative to an etch process from Chung et al., b) apply that teaching to the *thermal* oxidation of Thomas in which no regulation of oxidation rate is taught, and c) emerge with control of oxidation rate during *plasma* oxidation by regulation of reaction kinetics, as recited in the claims.

The references cannot be combined, there is no motivation to combine the references, and the combined references fail to teach each and every limitations of the claims.

Accordingly, Appellants respectfully request that the rejections of claims 72, 89, 96, 103, and 108 and their dependent claims be withdrawn.

CONCLUSION

Accordingly, Appellants respectfully solicit the Honorable Board of Patent Appeals and Interferences to reverse the rejections of the pending claims and pass this application on to allowance.

Respectfully submitted,

Dec. 13, 2005

Date



Pamela J. Squyres
Reg. No. 52,246

Matrix Semiconductor, Inc.
3230 Scott Boulevard
Santa Clara, CA 95054
(408) 869-2921
(408) 869-8923 (fax)

VIII. CLAIMS APPENDIX

1. A plasma oxidation process comprising:
exposing an oxidizable surface to an oxidizing plasma,
wherein the oxidizing plasma has an activity relative to the oxidizable surface;
forming an oxide film on the oxidizable surface; and
regulating the oxidizing plasma activity to limit a rate of formation of the oxide film.
2. The plasma oxidation process of claim 1, wherein regulating the oxidizing plasma activity comprises bombarding the oxidizable surface with energized ions prior to exposing the oxidizable surface to the oxidizing plasma.
3. The plasma oxidation process of claim 2, wherein bombarding the oxidizable surface comprises bombarding the oxidizable surface to remove contaminants from the oxidizable surface.
4. The plasma oxidation process of claim 2, wherein bombarding the oxidizable surface comprises bombarding the oxidizable surface to remove other oxide layers present on the oxidizable surface.
5. The plasma oxidation process of claim 2, wherein bombarding the oxidizable surface comprises bombarding the oxidizable surface to facet the oxidizable surface.
6. The plasma oxidation process of claim 2, wherein bombarding the oxidizable surface with energized ions comprises subjecting the oxidizable surface to a bias voltage.
7. The plasma oxidation process of claim 1, wherein regulating the oxidizing plasma activity comprises diluting the oxidizing plasma with an inert gas.
8. The plasma oxidation process of claim 1 further comprising providing a substrate having a back surface opposite a face surface, wherein the oxidizable surface comprises at least a portion of the face surface, and wherein regulating the oxidizing plasma activity comprises contacting the back surface with a cooling medium.

9. The plasma oxidation process of claim 1, wherein regulating the oxidizing plasma activity comprises applying an RF bias voltage to the oxidizable surface.
10. The plasma oxidation process of claim 1 further comprising:
providing a plasma chamber;
placing a substrate in the plasma chamber; and
igniting the oxidizing plasma after placing the substrate in the plasma chamber.
11. The plasma oxidation process of claim 1 further comprising igniting an inert gas plasma prior to igniting the oxidizing plasma.
12. The plasma oxidation process of claim 11 further comprising placing the oxidizable surface in the inert gas plasma.
13. The plasma oxidation process of claim 1 further comprising providing a plasma power source having an output power, and wherein regulating the oxidizing plasma comprises limiting the output power to a predetermined level.
14. The plasma oxidation process of claim 1, wherein the oxidizable surface comprises silicon.
15. The plasma oxidation process of claim 1, wherein the oxidizable surface comprises a semiconductor element of an antifuse device.
16. The plasma oxidation process of claim 1, wherein exposing an oxidizable surface to an oxidizing plasma comprises exposing the oxidizable surface to a plasma comprising oxygen.
17. The plasma oxidation process of claim 1, wherein regulating the oxidizing plasma activity comprises applying a bias voltage and sputtering a portion of the oxide film while simultaneously forming the oxide film.

18. A process for fabricating an oxide film in a semiconductor device comprising the steps of:
 - forming a semiconductor layer;
 - exposing the semiconductor layer to a plasma comprising oxygen, wherein the plasma has an activity relative to the semiconductor layer;
 - forming an oxide film on the semiconductor layer; and
 - regulating the plasma activity to limit a rate of formation of the oxide film.
19. The process of claim 18, wherein the step of forming a semiconductor layer comprises forming a doped semiconductor layer.
20. The process of claim 18, wherein the step of forming a semiconductor layer comprises forming a silicon layer.
21. The process of claim 18, wherein the step of forming a semiconductor layer comprises forming a germanium layer.
22. The process of claim 18 further comprising forming an electrically conductive layer prior to forming the semiconductor layer.
23. The process of claim 18, wherein the oxide film comprises a gate oxide layer.
24. The process of claim 18, wherein the oxide film comprises a passivation layer.
- 25-34. (Withdrawn)
35. A process for forming an antifuse comprising:
 - exposing an oxidizable surface to a plasma oxidation process for an initial exposure time; and
 - growing an oxide film on the oxidizable surface, and

wherein the oxide film grows to a predetermined thickness at an end of the initial exposure time, and wherein additional exposure to the plasma oxidation process beyond the initial exposure time does not result in a significant further increase in thickness of the oxide film.

36. The process of claim 35, wherein the plasma oxidation process comprises providing a substrate having a back surface opposite a face surface, wherein the oxidizable surface comprises at least a portion of the face surface, and contacting the back surface with a cooling medium.

37. The process of claim 35, wherein the plasma oxidation process comprises applying an RF bias voltage to the oxidizable surface.

38. The process of claim 35, wherein the plasma oxidation process comprises generating a plasma comprising oxygen and an inert gas.

39. The process of claim 35, further comprising subjecting the oxidizable surface to a plasma containing a nitrogen species prior to exposing the oxidizable surface to a plasma oxidation process.

40. The process of claim 39, wherein subjecting the oxidizable surface to a plasma containing a nitrogen species comprises subjecting the oxidizable surface to a plasma formed by a gas selected from the group consisting of nitrogen, nitrous oxide and ammonia.

41-54. (Withdrawn)

55. A process for fabricating a dielectric film in a semiconductor device comprising the steps of:

exposing an oxidizable surface to a plasma comprising an oxygen species and a nitrogen species,

wherein the plasma has an activity relative to the oxidizable surface;

forming an oxynitride film on the oxidizable surface; and

regulating the plasma activity to limit a rate of formation of the oxynitride film.

56. The process of claim 55, wherein the nitrogen species comprises a compound selected from the group consisting of nitrogen, ammonia and nitrous oxide.

57. The process of claim 55, wherein the step of forming an oxynitride film comprises a gate oxide layer.

58. The process of claim 55, wherein the step of forming an oxynitride film comprises a passivation layer.

59. The process of claim 55, wherein the step of forming an oxynitride film comprises an antifuse layer.

60. The process of claim 55, further comprising subjecting the oxidizable surface to a plasma containing a nitrogen species prior to exposing the oxidizable surface to a plasma comprising an oxygen species and a nitrogen species.

61. The process of claim 60, wherein subjecting the oxidizable surface to a plasma containing a nitrogen species comprises subjecting the oxidizable surface to a plasma formed by a gas selected from the group consisting of nitrogen, nitrous oxide and ammonia.

62. A process for fabricating an oxide film in a semiconductor device comprising the steps of:

exposing an oxidizable surface to a plasma comprising oxygen,
wherein the plasma has an activity relative to the oxidizable surface;
forming an oxide film on the oxidizable surface;
regulating the plasma activity to limit a rate of formation of the oxide film; and
forming a silicon nitride layer overlying the oxide film.

63. The process of claim 62, wherein the step of forming a silicon nitride layer comprises plasma deposition of silicon nitride.

64. The process of claim 62, wherein the step of forming a silicon nitride layer comprises chemical vapor deposition of silicon nitride.
65. The process of claim 62, further comprising subjecting the oxidizable surface to a plasma containing a nitrogen species prior to exposing the oxidizable surface to a plasma comprising oxygen.
66. The process of claim 65, wherein subjecting the oxidizable surface to a plasma containing a nitrogen species comprises subjecting the oxidizable surface to a plasma formed by a gas selected from the group consisting of nitrogen, nitrous oxide and ammonia.
67. A process for fabricating a dielectric film in a semiconductor device comprising the steps of:
 - exposing an oxidizable surface to a plasma comprising an oxygen species, wherein the plasma has an activity relative to the oxidizable surface;
 - forming an oxide film having an upper surface on the oxidizable surface;
 - regulating the plasma activity to limit a rate of formation of the oxide film; and
 - forming an oxynitride region at the upper surface of the oxide film.
68. The process of claim 67, wherein the step of forming an oxynitride region comprises subjecting the oxide film to a plasma containing a nitrogen species.
69. The process of claim 68, wherein subjecting the oxide film to a plasma containing a nitrogen species comprises subjecting the oxide film to a plasma formed by a gas selected from the group consisting of nitrogen, nitrous oxide and ammonia.
70. The process of claim 67, further comprising subjecting the oxidizable surface to a plasma containing a nitrogen species prior to exposing the oxidizable surface to a plasma comprising oxygen.

71. The process of claim 70, wherein subjecting the oxidizable surface to a plasma containing a nitrogen species comprises subjecting the oxidizable surface to a plasma formed by a gas selected from the group consisting of nitrogen, nitrous oxide and ammonia.

72. A plasma oxidation process comprising:
exposing an oxidizable surface to an oxidizing plasma,
wherein the oxidizing plasma has an activity relative to the oxidizable surface;
forming an oxide film on the oxidizable surface; and
regulating the oxidizing plasma activity to limit a rate of formation of the oxide film by regulating at least one of the following: reaction kinetics, growth initiation, and surface energy.

73. The plasma oxidation process of claim 72, wherein regulating the oxidizing plasma activity comprises bombarding the oxidizable surface with energized ions prior to exposing the oxidizable surface to the oxidizing plasma.

74. The plasma oxidation process of claim 73, wherein bombarding the oxidizable surface comprises bombarding the oxidizable surface to remove contaminants from the oxidizable surface.

75. The plasma oxidation process of claim 73, wherein bombarding the oxidizable surface comprises bombarding the oxidizable surface to remove other oxide layers present on the oxidizable surface.

76. The plasma oxidation process of claim 73, wherein bombarding the oxidizable surface comprises bombarding the oxidizable surface to facet the oxidizable surface.

77. The plasma oxidation process of claim 73, wherein bombarding the oxidizable surface with energized ions comprises subjecting the oxidizable surface to a bias voltage.

78. The plasma oxidation process of claim 72, wherein regulating the oxidizing plasma activity comprises diluting the oxidizing plasma with an inert gas.

79. The plasma oxidation process of claim 72 further comprising providing a substrate having a back surface opposite a face surface, wherein the oxidizable surface comprises at least a portion of the face surface, and wherein regulating the oxidizing plasma activity comprises contacting the back surface with a cooling medium.
80. The plasma oxidation process of claim 72, wherein regulating the oxidizing plasma activity comprises applying an RF bias voltage to the oxidizable surface.
81. The plasma oxidation process of claim 72 further comprising:
 - providing a plasma chamber;
 - placing a substrate in the plasma chamber; and
 - igniting the oxidizing plasma after placing the substrate in the plasma chamber.
82. The plasma oxidation process of claim 72 further comprising igniting an inert gas plasma prior to igniting the oxidizing plasma.
83. The plasma oxidation process of claim 82 further comprising placing the oxidizable surface in the inert gas plasma.
84. The plasma oxidation process of claim 72 further comprising providing a plasma power source having an output power, and wherein regulating the oxidizing plasma comprises limiting the output power to a predetermined level.
85. The plasma oxidation process of claim 72, wherein the oxidizable surface comprises silicon.
86. The plasma oxidation process of claim 72, wherein the oxidizable surface comprises a semiconductor element of an antifuse device.

87. The plasma oxidation process of claim 72, wherein exposing an oxidizable surface to an oxidizing plasma comprises exposing the oxidizable surface to a plasma comprising oxygen.

88. The plasma oxidation process of claim 72, wherein regulating the oxidizing plasma activity comprises applying a bias voltage and sputtering a portion of the oxide film while simultaneously forming the oxide film.

89. A process for fabricating an oxide film in a semiconductor device comprising the steps of:

forming a semiconductor layer;
exposing the semiconductor layer to a plasma comprising oxygen,
wherein the plasma has an activity relative to the semiconductor layer;
forming an oxide film on the semiconductor layer; and
regulating the plasma activity to limit a rate of formation of the oxide film by
regulating at least one of the following: reaction kinetics, growth initiation, and surface energy.

90. The process of claim 89, wherein the step of forming a semiconductor layer comprises forming a doped semiconductor layer.

91. The process of claim 89, wherein the step of forming a semiconductor layer comprises forming a silicon layer.

92. The process of claim 89, wherein the step of forming a semiconductor layer comprises forming a germanium layer.

93. The process of claim 89 further comprising forming an electrically conductive layer prior to forming the semiconductor layer.

94. The process of claim 89, wherein the oxide film comprises a gate oxide layer.

95. The process of claim 89, wherein the oxide film comprises a passivation layer.
96. A process for fabricating a dielectric film in a semiconductor device comprising the steps of:
 - exposing an oxidizable surface to a plasma comprising an oxygen species and a nitrogen species,
 - wherein the plasma has an activity relative to the oxidizable surface;
 - forming an oxynitride film on the oxidizable surface; and
 - regulating the plasma activity to limit a rate of formation of the oxynitride film by regulating at least one of the following: reaction kinetics, growth initiation, and surface energy.
97. The process of claim 96, wherein the nitrogen species comprises a compound selected from the group consisting of nitrogen, ammonia and nitrous oxide.
98. The process of claim 96, wherein the step of forming an oxynitride film comprises a gate oxide layer.
99. The process of claim 96, wherein the step of forming an oxynitride film comprises a passivation layer.
100. The process of claim 96, wherein the step of forming an oxynitride film comprises an antifuse layer.
101. The process of claim 96, further comprising subjecting the oxidizable surface to a plasma containing a nitrogen species prior to exposing the oxidizable surface to a plasma comprising an oxygen species and a nitrogen species.
102. The process of claim 101, wherein subjecting the oxidizable surface to a plasma containing a nitrogen species comprises subjecting the oxidizable surface to a plasma formed by a gas selected from the group consisting of nitrogen, nitrous oxide and ammonia.

103. A process for fabricating an oxide film in a semiconductor device comprising the steps of:

exposing an oxidizable surface to a plasma comprising oxygen,
wherein the plasma has an activity relative to the oxidizable surface;
forming an oxide film on the oxidizable surface;
regulating the plasma activity to limit a rate of formation of the oxide film by
regulating at least one of the following: reaction kinetics, growth initiation, and surface
energy; and
forming a silicon nitride layer overlying the oxide film.

104. The process of claim 103, wherein the step of forming a silicon nitride layer
comprises plasma deposition of silicon nitride.

105. The process of claim 103, wherein the step of forming a silicon nitride layer
comprises chemical vapor deposition of silicon nitride.

106. The process of claim 103, further comprising subjecting the oxidizable surface to a
plasma containing a nitrogen species prior to exposing the oxidizable surface to a plasma
comprising oxygen.

107. The process of claim 106, wherein subjecting the oxidizable surface to a plasma
containing a nitrogen species comprises subjecting the oxidizable surface to a plasma formed
by a gas selected from the group consisting of nitrogen, nitrous oxide and ammonia.

108. A process for fabricating a dielectric film in a semiconductor device comprising the
steps of:

exposing an oxidizable surface to a plasma comprising an oxygen species,
wherein the plasma has an activity relative to the oxidizable surface;
forming an oxide film having an upper surface on the oxidizable surface;
regulating the plasma activity to limit a rate of formation of the oxide film by
regulating at least one of the following: reaction kinetics, growth initiation, and surface
energy; and

forming an oxynitride region at the upper surface of the oxide film.

109. The process of claim 108, wherein the step of forming an oxynitride region comprises subjecting the oxide film to a plasma containing a nitrogen species.

110. The process of claim 109, wherein subjecting the oxide film to a plasma containing a nitrogen species comprises subjecting the oxide film to a plasma formed by a gas selected from the group consisting of nitrogen, nitrous oxide and ammonia.

111. The process of claim 108, further comprising subjecting the oxidizable surface to a plasma containing a nitrogen species prior to exposing the oxidizable surface to a plasma comprising oxygen.

112. The process of claim 111, wherein subjecting the oxidizable surface to a plasma containing a nitrogen species comprises subjecting the oxidizable surface to a plasma formed by a gas selected from the group consisting of nitrogen, nitrous oxide and ammonia.

113. A plasma oxidation process comprising:
exposing an oxidizable surface to an oxidizing plasma,
wherein the oxidizing plasma has an activity relative to the oxidizable surface;
forming an oxide film on the oxidizable surface; and
regulating the oxidizing plasma activity to limit a rate of formation of the oxide film to a predetermined growth rate while the oxidizable surface is being exposed to the oxidizing plasma.

114. The plasma oxidation process of claim 113, wherein regulating the oxidizing plasma activity comprises bombarding the oxidizable surface with energized ions prior to exposing the oxidizable surface to the oxidizing plasma.

115. The plasma oxidation process of claim 114, wherein bombarding the oxidizable surface comprises bombarding the oxidizable surface to remove contaminants from the oxidizable surface.

116. The plasma oxidation process of claim 114, wherein bombarding the oxidizable surface comprises bombarding the oxidizable surface to remove other oxide layers present on the oxidizable surface.
117. The plasma oxidation process of claim 114, wherein bombarding the oxidizable surface comprises bombarding the oxidizable surface to facet the oxidizable surface.
118. The plasma oxidation process of claim 114, wherein bombarding the oxidizable surface with energized ions comprises subjecting the oxidizable surface to a bias voltage.
119. The plasma oxidation process of claim 113, wherein regulating the oxidizing plasma activity comprises diluting the oxidizing plasma with an inert gas.
120. The plasma oxidation process of claim 113 further comprising providing a substrate having a back surface opposite a face surface, wherein the oxidizable surface comprises at least a portion of the face surface, and wherein regulating the oxidizing plasma activity comprises contacting the back surface with a cooling medium.
121. The plasma oxidation process of claim 113, wherein regulating the oxidizing plasma activity comprises applying an RF bias voltage to the oxidizable surface.
122. The plasma oxidation process of claim 113 further comprising:
 - providing a plasma chamber;
 - placing a substrate in the plasma chamber; and
 - igniting the oxidizing plasma after placing the substrate in the plasma chamber.
123. The plasma oxidation process of claim 113 further comprising igniting an inert gas plasma prior to igniting the oxidizing plasma.
124. The plasma oxidation process of claim 123 further comprising placing the oxidizable surface in the inert gas plasma.

125. The plasma oxidation process of claim 113 further comprising providing a plasma power source having an output power, and wherein regulating the oxidizing plasma comprises limiting the output power to a predetermined level.
126. The plasma oxidation process of claim 113, wherein the oxidizable surface comprises silicon.
127. The plasma oxidation process of claim 113, wherein the oxidizable surface comprises a semiconductor element of an antifuse device.
128. The plasma oxidation process of claim 113, wherein exposing an oxidizable surface to an oxidizing plasma comprises exposing the oxidizable surface to a plasma comprising oxygen.
129. The plasma oxidation process of claim 113, wherein regulating the oxidizing plasma activity comprises applying a bias voltage and sputtering a portion of the oxide film while simultaneously forming the oxide film.
130. A process for fabricating an oxide film in a semiconductor device comprising the steps of:
 - forming a semiconductor layer;
 - exposing the semiconductor layer to a plasma comprising oxygen, wherein the plasma has an activity relative to the semiconductor layer;
 - forming an oxide film on the semiconductor layer; and
 - regulating the plasma activity to limit a rate of formation of the oxide film to a predetermined growth rate while the semiconductor layer is being exposed to the plasma.
131. The process of claim 130, wherein the step of forming a semiconductor layer comprises forming a doped semiconductor layer.

132. The process of claim 130, wherein the step of forming a semiconductor layer comprises forming a silicon layer.
133. The process of claim 130, wherein the step of forming a semiconductor layer comprises forming a germanium layer.
134. The process of claim 130 further comprising forming an electrically conductive layer prior to forming the semiconductor layer.
135. The process of claim 130, wherein the oxide film comprises a gate oxide layer.
136. The process of claim 130, wherein the oxide film comprises a passivation layer.
137. A process for fabricating a dielectric film in a semiconductor device comprising the steps of:
 - exposing an oxidizable surface to a plasma comprising an oxygen species and a nitrogen species,
 - wherein the plasma has an activity relative to the oxidizable surface;
 - forming an oxynitride film on the oxidizable surface; and
 - regulating the plasma activity to limit a rate of formation of the oxynitride film to a predetermined growth rate while the oxidizable surface is being exposed to the plasma.
138. The process of claim 137, wherein the nitrogen species comprises a compound selected from the group consisting of nitrogen, ammonia and nitrous oxide.
139. The process of claim 137, wherein the step of forming an oxynitride film comprises a gate oxide layer.
140. The process of claim 137, wherein the step of forming an oxynitride film comprises a passivation layer.

141. The process of claim 137, wherein the step of forming an oxynitride film comprises an antifuse layer.

142. The process of claim 137, further comprising subjecting the oxidizable surface to a plasma containing a nitrogen species prior to exposing the oxidizable surface to a plasma comprising an oxygen species and a nitrogen species.

143. The process of claim 142, wherein subjecting the oxidizable surface to a plasma containing a nitrogen species comprises subjecting the oxidizable surface to a plasma formed by a gas selected from the group consisting of nitrogen, nitrous oxide and ammonia.

144. A process for fabricating an oxide film in a semiconductor device comprising the steps of:

exposing an oxidizable surface to a plasma comprising oxygen,
wherein the plasma has an activity relative to the oxidizable surface;
forming an oxide film on the oxidizable surface;
regulating the plasma activity to limit a rate of formation of the oxide film to a predetermined growth rate while the oxidizable surface is being exposed to the plasma; and
forming a silicon nitride layer overlying the oxide film.

145. The process of claim 144, wherein the step of forming a silicon nitride layer comprises plasma deposition of silicon nitride.

146. The process of claim 144, wherein the step of forming a silicon nitride layer comprises chemical vapor deposition of silicon nitride.

147. The process of claim 144, further comprising subjecting the oxidizable surface to a plasma containing a nitrogen species prior to exposing the oxidizable surface to a plasma comprising oxygen.

148. The process of claim 147, wherein subjecting the oxidizable surface to a plasma containing a nitrogen species comprises subjecting the oxidizable surface to a plasma formed by a gas selected from the group consisting of nitrogen, nitrous oxide and ammonia.

149. A process for fabricating a dielectric film in a semiconductor device comprising the steps of:

exposing an oxidizable surface to a plasma comprising an oxygen species,
wherein the plasma has an activity relative to the oxidizable surface;
forming an oxide film having an upper surface on the oxidizable surface;
regulating the plasma activity to limit a rate of formation of the oxide film to a predetermined growth rate while the oxidizable surface is being exposed to the plasma; and
forming an oxynitride region at the upper surface of the oxide film.

150. The process of claim 149, wherein the step of forming an oxynitride region comprises subjecting the oxide film to a plasma containing a nitrogen species.

151. The process of claim 150, wherein subjecting the oxide film to a plasma containing a nitrogen species comprises subjecting the oxide film to a plasma formed by a gas selected from the group consisting of nitrogen, nitrous oxide and ammonia.

152. The process of claim 149, further comprising subjecting the oxidizable surface to a plasma containing a nitrogen species prior to exposing the oxidizable surface to a plasma comprising oxygen.

153. The process of claim 152, wherein subjecting the oxidizable surface to a plasma containing a nitrogen species comprises subjecting the oxidizable surface to a plasma formed by a gas selected from the group consisting of nitrogen, nitrous oxide and ammonia.

Serial Number 09/918,853

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.